AMENDMENTS TO THE CLAIMS

1. (Canceled).

2. (Currently Amended) The device of claim [[1]] 18, wherein the validation circuit indicates when the sense amplifier has sufficiently settled on a sensed condition of the buried fuse.

3. (Previously Amended) The device of claim 2, further comprising:

a power control circuit for powering the buried fuse reading device up and down; and wherein

the validation circuit indicates when the sense amplifier has sufficiently settled on a sensed condition once the power control circuit begins powering up the buried fuse reading device.

4. (Original) The device of claim 3, further comprising:

a bias generating circuit for generating first and second voltages; and wherein

the sense amplifier operates based on the first and second voltages.

5. (Original) The device of claim 4, wherein the validation circuit operates based on the first and second voltages.

6. (Original) The device of claim 5, wherein

the sense amplifier includes a first PMOS transistor and a first NMOS transistor connected in series with the buried fuse, a gate of the first PMOS transistor receiving the first voltage and a gate of the first NMOS transistor receiving the second voltage; and

the validation circuit includes a second PMOS transistor and a second NMOS transistor connected in series, a gate of the second PMOS transistor receiving the first voltage and a gate of the second NMOS transistor receiving the second voltage, the second PMOS and NMOS transistor being weaker than the first PMOS and NMOS transistor, respectively.

7. (Currently Amended) The device of claim [[1]] 18, comprising:

a plurality of buried fuses; and

a sense amplifier associated with each of the buried fuses.

8. (Currently Amended) [[A]] The ~~buried fuse reading~~ device of claim 18, ~~comprising:~~

~~at least one buried fuse;~~

~~at least one sense amplifier sensing a condition of the buried fuse; and~~

~~a~~ wherein, the validation circuit dynamically ~~adjusting~~ adjusts a validation point based on the sense amplifier operating conditions, the validation point being a point in time when the sense amplifier output is considered valid.

9. (Original) The device of claim 8, further comprising:

a power control circuit for powering the buried fuse reading device up and down; and wherein

the validation point is the point in time when output from the sense amplifier is considered valid once the power control circuit begins powering up the buried fuse reading device.

10. (Original) The device of claim 9, further comprising:

a bias generating circuit for generating first and second voltages; and wherein

the sense amplifier operates based on the first and second voltages.

11. (Original) The device of claim 10, wherein the validation circuit operates based on the first and second voltages.

12. (Original) The device of claim 11, wherein

the sense amplifier includes a first PMOS transistor and a first NMOS transistor connected in series with the buried metal fuse, a gate of the first PMOS transistor receiving the first voltage and a gate of the first NMOS transistor receiving the second voltage; and

the validation circuit includes a second PMOS transistor and a second NMOS transistor connected in series, a gate of the second PMOS transistor receiving the first voltage and a gate of the second NMOS transistor receiving the second voltage, the second PMOS and NMOS transistor being weaker than the first PMOS and NMOS transistor, respectively.

13. (Original) The device of claim 8, comprising:

a plurality of buried fuses; and

a sense amplifier associated with each of the buried fuses.

14. (Canceled).

15. (Currently Amended) The device of claim [[14]] 18, comprising:

a power control circuit for powering the buried fuse reading device up and down.

16. (Currently Amended) The device of claim 15, wherein the sense amplifier and the ~~tracking~~ validation circuit draw substantially no current when the power control circuit has the buried fuse reading device powered down.

17. (Previously Presented) A buried fuse reading device, comprising:

a buried fuse;

a sense amplifier including a first PMOS transistor and a first NMOS transistor connected in series with the buried fuse, a gate of the first PMOS transistor receiving a first voltage and a gate of the first NMOS transistor receiving a second voltage; and

a validation circuit including a second PMOS transistor and a second NMOS transistor connected in series, a gate of a second PMOS transistor receiving the first voltage and a gate of a second NMOS transistor receiving the second voltage, the second PMOS transistor and second NMOS transistor being weaker than the first PMOS transistor and first NMOS transistor, respectively.

18. (Previously Presented) A buried fuse reading device, comprising:

at least one buried fuse;

at least one sense amplifier sensing a condition of the buried fuse; and

a validation circuit mimicking, with a delay, the sense amplifier regardless of the state of the at least one buried fuse, and indicating when the sense amplifier output is valid.

19. (Currently Amended) The device of claim 18, wherein the validation circuit is the same as the at least one sense amplifier ~~but for the delay in the validation circuit~~ except that the validation circuit includes weaker components.

20 (Previously Presented) The device of claim 18, wherein the validation circuit is connected in parallel with the at least one sense amplifier and the at least one buried fuse.